Curriculum Vitae

TAE-HWAN KIM

DMC R&D Center
Samsung Electronics

416, Maetan-dong, Youngtong-gu
Suwon, Kyungki-do,153-030, Korea
+82-10-9953-7098
bestcorean@gmail.com

EDUCATION:

Ph.D. Electrical Engineering,
KAIST, Daejeon, Korea (Feb. 23, 2007 ~ Aug. 20, 2010)
M.S. Electrical Engineering,
KAIST, Daejeon, Korea (Mar.1, 2005 ~ Feb. 2, 2007)
B.S. Electrical Engineering,
YONSEI University, Seoul, Korea, (Mar. 2, 1998 ~ Feb. 28, 2005)
Graduation with High Honors

AWARDS & HONORS:

1. Best Ph. D. Thesis, KAIST
   - Feb. 11, 2011
2. Awards for Excellence in Research (3-times), Dept. EE, KAIST
   - April 3, 2008
   - April 6, 2009
   - April 8, 2010
3. IP Design Contest - Bronze Medal (3rd place), Korea Intellectual Property Office
   - Tae-Hwan Kim and Young-Joo Lee
   - Dec. 8, 2008
4. IP Design Contest - Best Design Award (1st place), Dongbu Hitek
   - Ji-Hoon Kim, Tae-Hwan Kim, and Hae-Soo Jeon
   - July 23, 2007
5. Graduation with High Honors, YONSEI University
   - Feb. 28, 2005

RESEARCH INTERESTS:

- VLSI Architectures for DSP Systems
  - MIMO-OFDM Receivers: Detection & Synchronization
  - Sound Synthesis Systems
  - Digital Correction of Optical Distortion
- General-purpose Microprocessor Architectures
  - Multiprocessor Architectures for Embedded Applications
  - Memory System Architectures

RELEVANT COURSEWORK:

- Computer System & Microprocessor Architecture, S.o.C. Architecture, Digital Logic Design,

VLSI, Digital Integrated Circuits, Computer Arithmetic, Digital Signal Processing, Wireless Communication Systems, etc.

PUBLICATIONS:

INTERNATIONAL JOURNALS:

J1. Tae-Hwan Kim and In-Cheol Park, “Efficient Pruning for Infinity-norm Sphere Decoding,” *IEICE Transactions on Communications*. [To be published]

J2. In-Cheol Park and Tae-Hwan Kim, “Multiplier-less and Table-less Linear Approximation for Square-related Functions,” *IEICE Transactions on Information & Systems*, vol. e93-d, no. 11, pp. 2979-2988, Nov. 2010.

J3. Tae-Hwan Kim and In-Cheol Park, "Small-Area and Low-Energy *K*-Best MIMO Detector Using Relaxed Tree Expansion and Early Forwarding," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 10, pp. 2753-2761, Oct. 2010.

J4. Tae-Hwan Kim and In-Cheol Park, "High-throughput and Area-efficient MIMO Symbol Detection Based on Modified Dijkstra's Search," *IEEE Transactions on Circuits and Systems I:Regular Papers*, vol. 57, no. 7, pp. 1756-1766, July 2010.

J5. Tae-Hwan Kim, Young-Joo Lee, and In-Cheol Park, "Design of a Scalable and Programmable Sound Synthesizer," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 18, no. 6, pp. 875-886, June 2010.

J6. Tae-Hwan Kim and In-Cheol Park, " Low-power and High-accurate Synchronization for IEEE 802.16d Systems," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 16, no. 12, pp. 1620-1630, Dec. 2008.

INTERNATIONAL CONFERENCES:

C1. Tae-Hwan Kim and In-Cheol Park, “A 2.6Gb/s 1.56mm² Near-Optimal MIMO Detector in 0.18μm CMOS,” *Custom Integrated Circuits Conference* (CICC), pp. 1-4, Sept. 2010.

C2. Tae-Hwan Kim and In-Cheol Park, "Small-Area and Low-Energy *K*-Best MIMO Detector Using Relaxed Tree Expansion and Early Forwarding," *International Symposium on Low Power Electronics and Design* (ISLPED), pp. 231-236, Aug. 2010.

C3. In-Cheol Park and Tae-Hwan Kim, "Multiplier-less and Table-less Linear Approximation for Square and Square-root," *IEEE International Conference on Computer Design* (ICCD), pp. 378-383, Oct. 2009.

C4. Tae-Hwan Kim and In-Cheol Park, "Implementation of a High-throughput and Area-efficient MIMO Detector Based on Modified Dijkstra's Search," *IEEE Global Communication Conference* (GLOBECOM), pp. 1-6, Nov. 2009.

C5. Tae-Hwan Kim, Young-Joo Lee, and In-Cheol Park, "A Scalable and Programmable Sound Synthesizer," *IEEE International Symposium on Circuits and Systems* (ISCAS), pp. 1855-1858, May 2009.

C6. Tae-Hwan Kim, Young-Joo Lee and In-Cheol Park, "Design of a Scalable Sound Synthesizer," *IEEE International SoC Design Conference* (ISOCC), vol. 03, pp. 56-57, Nov. 2008.

C7. Tae-Hwan Kim and In-Cheol Park, "Time-domain Joint Estimation of Fine Symbol Timing Offset and Integer Carrier Frequency Offset" *IEEE Vehicular Technology Conference* (VTC), pp. 1186-1190, May 2008.

C8. Tae-Hwan Kim and In-Cheol Park, "Area and Power Efficient Design of Coarse Time Synchronizer and Frequency Offset Estimator for Fixed WiMAX Systems" *13th Asia and South Pacific Design Automation Conference* (ASP-DAC), pp. 111-112, Mar. 2008.

C9. Tae-Hwan Kim and In-Cheol Park, "Two-step Approach for Coarse Time Synchronization and Frequency Offset Estimation for IEEE 802.16D Systems," *IEEE Workshop on Signal Processing Systems* (SiPS), pp. 193-198, Oct. 2007.

DOMESTIC CONFERENCES:

D1. Eun-Chan Kim, Bong-Jin Kim, Tae-Hwan Kim, and In-Cheol Park, "Coherence Management Unit Saving Modified Lines Internally for Multicore System," *IEEK Summer Conference*, vol. 33, no. 1, pp. 1564-1566, April 2010.

D2. Young-Joo Lee, Tae-Hwan Kim, Kang-Woo Park, Go-Eun Lim, and In-Cheol Park, "A Fully-integrated Reader System for Mobile UHF RFID," *Korean Conference on Semiconductors* (KCS 2010).

D3. Tae-Hwan Kim and In-Cheol Park, "Area-efficient Architecture for Joint Estimation of Fine Timing and Integer Carrier Frequency Offsets," *Korean Conference on Semiconductors* (KCS 2007).

PATENTS:

P1. Tae-Hwan Kim and In-Cheol Park, "Description of Combinational Logics Using Spreadsheet Program and Automatic Conversion Tool," Korea 10-0907224.

P2. Tae-Hwan Kim, Young-Joo Lee, and In-Cheol Park, "Apparatus of Supporting Delay Access, Method of Supporting Delay Access and Sound Synthesis Apparatus of Supporting Delay Access," Korea 10-0941081.

P3. Tae-Hwan Kim, Young-Joo Lee, and In-Cheol Park, "Programmable Sound Synthesis Apparatus and Programmable Sound Synthesis Method," Korea 10-2008-0049065.

P4. Tae-Hwan Kim, Eun-Chan Kim, Bong-Jin Kim, and In-Cheol Park, “Multi-core Cache Circuit Using Single-core Cache Controller, Cache Device and Semiconductor Device Including the Same, and method for Controlling the Cache Memory,” Korea 10-2010-0006038.

P5. [Pended] Bong-Jin Kim, Tae-Hwan Kim, Eun-Chan Kim, and In-Cheol Park, “Apparatus for Controlling Memory Management Unit, Multi-core Processor and Computer System Including the Same, and Method of Controlling Memory Management Unit,” Korea 10-2010-0006031.

P6. [Pended] Eun-Chan Kim, Bong-Jin Kim, Tae-Hwan Kim, and In-Cheol Park, “Method for Managing Coherence, Coherence Management Unit, Cache Device and Semiconductor Device Including the Same,” Korea 10-2010-0011423.

P7. [Pended] Tae-Hwan Kim and In-Cheol Park, “Lens Distortion Correction Device Using Lens Identification Number, Camera Employing the Same and Method for Correcting Lens Distortion,” Korea 10-2010-0032083.

EMPLOYMENT:

- Senior Research Engineer
  - DMC R&D Center, Samsung Electronics Co. Ltd., Suwon, Korea
  - Aug. 1, 2010 ~ Present
  - Research and development of DSP systems for WLAN
- Teaching and Research Assistant
  - Dept. EE, KAIST, Daejeon, Korea
  - Feb. 23, 2005 ~ Aug. 31, 2010
- Software Developer
  - Cyber-R.com, Seoul, Korea
  - Feb. 14, 2001 ~ Feb. 15, 2004
  - Development of server-side applications

PROFESSIONAL ACTIVITIES:

- IEEE Associate Member
  - Aug. 2010 ~ Present
- IEEE Student Member
  - Feb. 2006 ~ Aug. 2010

PROJECTS (HARDWARE DEVELOPMENT):

- Multi-core Cache Design
  - Aug. 2009 ~ Dec. 2009, Sponsored by Korea Intellectual Property Office
  - Project leader
  - The goal of this project was to develop a cache controller to support multi-core processors. I designed and implemented a cache controller supporting up to 4 cores. Each cache was based on 4-way set-associative with pseudo-LRU replacement policy, and the coherence between the caches was managed according to MESI protocol.
- 2nd gen. 32-bit Embedded Processor Design (Core-A²)
  - Feb. 2009 ~ Dec. 2009, Sponsored by Korea Intellectual Property Office
  - Project leader
  - The goal of this project was to develop a new RISC processor targeting high-performance embedded applications. I designed an entire architecture for the embedded processor named as Core-A². Compared with its former version, Core-A, Core-A² supported several new features such as SIMD operations and memory synchronization.
- Hybrid Sound Synthesizer Design
  - Feb. 2008 ~ June. 2008, Sponsored by Korea Intellectual Property Office
  - Project leader
  - I developed a sound synthesis system by proposing a new scalable architecture. Two heterogeneous RISC processors were integrated in the system: one of them is a sound synthesis processor that was designed by defining a new ISA optimized for realizing a programmable data-flow of sound synthesis algorithms; the other is a general-purpose embedded processor, Core-A, that was optimized for interpreting MIDI data. I designed and implemented the entire hardware system from scratch to silicon. The system was verified on a FPGA-based system, and fabricated as an ASIC, finally.
- RFID Baseband Modem Design
  - Jan. 2007 ~ Dec. 2007, Sponsored by SoCium
  - Project leader
  - I developed a baseband system targeting UHF RFID standard that was ratified as EPCglobal Generation-1 Class-1. The system integrated 16-bit embedded processor, baseband modem, and other peripherals including a UART and a GPIO. To achieve low-power consumption, a new ISA was designed for the embedded processor to efficiently handle the RFID protocols. The baseband modem was designed with an edge-adjusting scheme to achieve a robust data recovery. I developed the entire baseband system and its software development kits including an assembler and a simulator. The baseband system was integrated with an analog frontend, and the whole system was fabricated on one chip. The entire system was verified by interacting with commercial RFID tags.
- 32-bit Embedded Processor Design (Core-A)
  - Feb. 2006 ~ Dec. 2006, Sponsored by Korea Intellectual Property Office
  - The goal of this project was to develop a new RISC processor targeting high-performance embedded applications. I studied on famous embedded processor architectures such as ARM and MIPS, and worked for developing a new ISA for the embedded processor named as Core-A. I also developed an instruction set simulator for Core-A.
- Embedded System Development Platform

- Mar. 2005 ~ Dec. 2005, Sponsored by Ministry of Knowledge Economy
- The goal of this project was to develop a new embedded system platform. The platform included an embedded processor, on-chip bus, and other essential peripherals including interrupt controller and GPIO. I developed a GUI-based instruction set simulator for the embedded processor using GTK, and three AMBA-compatible peripherals: interrupt controller, GPIO, and UART.

PROJECTS (SOFTWARE DEVELOPMENT):

- Overlay Multicast Network Framework
  - Feb. 2004 ~ June. 2004, Research work in the undergraduate course
  - The goal of this project was to develop a virtual multi-cast network by overlaying the unicast network. I developed a UDP socket driver that overridden conventional unicast networks, and demonstrated the overlay network by implementing a video communication application based on RTP and H.263. In the overlay multicast network, the membership was centrally managed by a XML-based web-service via SOAP.
- HTTP 1.1 Compatible Web Server
  - Sept. 2004 ~ Dec. 2004, Term project in the OS class.
  - The web server supported HTTP 1.1 standard. Each HTTP request was handled by a separate thread, and the thread creation overhead was minimized by employing a thread-pool. This experimental web-server was developed using POSIX synchronization primitives.
- XML-RPC Library
  - Sept. 2003~Dec. 2003, Sponsored by Cyber-R
  - XML-RPC is a famous RPC protocol which uses XML to package the invocation data. I developed a java library which provided functionalities required in XML-RPC messaging. The library supported run-time configurability of the XML parser which performed underlying XML processing, and its transport layer could also be configured to use any protocols including HTTP and TCP/IP.
- High-performance Server Application Framework
  - Jan. 2003~Sept. 2003, Sponsored by Cyber-R
  - The goal of this project was to develop a general server framework for achieving scalability and high-performance. The server architecture was basically staged-event-driven, and the latency-hiding technique was employed. Multiple threads were provided to serve multiple concurrent requests, and they were reused by employing a thread-pool. The database connection was simplified by using an object-relational mapping.
- Graphic UI Component Library
  - Jan. 2002~Dec. 2002, Sponsored by Cyber-R and SK-Telecom
  - MIDP (mobile information device profile) 1.0 in J2ME was very naïve in 2002. The profile did not define any high-level UI components in its graphic tool-kit. I developed several graphic UI components based on low-level graphic functions. The library was used to make several cell-phone applications commercialized by SK-Telecom.
- Web-application Framework
  - Feb. 2001~Dec. 2001, Sponsored by Cyber-R and CHB
  - The goal of this project was to develop a web-application framework based on Java servlet 2.1, and its architecture is basically MVC. In CHB, hundreds of banking services were developed using this framework I developed, and the total amount of their transaction was up to about 100M $ per day in 2001.

SKILLS:

- Hardware Design Skills:
  - Proficient at RTL Design Using Verilog HDL
  - RTL Simulation/Verification Using NCSim or Modelsim
  - Backend Semi-custom Design Using Synopsys Tools Including
    Astro, Design-compiler, Prime-time, Formality, and Power-compiler
  - Circuit Design Using PSpice or HSpice
  - FPGA Design Using ALTERA's Quartus
- Software Design Skills:
  - Proficient at C/C++, Java, MATLAB
  - Multi-thread/Multi-process Programming
  - J2ME, J2EE
  - XML-related technologies including XML, XSD, XPATH, etc.
  - Distributed Processing: Web-service, Java-RMI, CORBA
  - JSP/ASP/PHP, Java-script, HTML
  - Various Libraries Including MFC and GTK

MISCELLANEOUS:

Military Service (Feb. 28, 2001 ~ Feb. 14, 2004)

REFERENCES:

Provided on request